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Implementation of an Efficient 14-Transistor Full Adder (.18µm technology) Using DTMOS

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Abstract: In day to day life the demand of portable electronic devices is increasing. These portable devices must work on low power and high speed. Low power VLSI circuits are the critical components to implement these portable devices. Speed is the major factor of these devices but there is always a trade-off between speed and power. DTMOS technology offers high speed but at the same time it consumes more power than CMOS. DTMOS also shows better results at low voltages. In this paper 1-bit and higher bits 14-T full adder circuits are implemented using DTMOS technology and compared with CMOS technology. From the results it can be concluded that DTMOS adder shows higher speed than CMOS.

Keywords: 14-transistor Full Adder, DTMOS, High speed, CMOS, Low Power.

I. INTRODUCTION

Many digital circuits and processors like DSPs use arithmetic equations to further process the information. Hence these arithmetic operations need to be faster and consume low power to process the instructions. Adder is the basic building block of every digital circuit so to make the calculations faster, adder circuit must be optimize. An adder circuit can be used by many different circuits like subtractors, multipliers and MAC (Multiply and accumulators). In this paper 1-bit, 4-bit, 8-bit and 16-bit full adder using 14-Transistors are made using both DTMOS and CMOS technology and then compared with each other. In many digital circuits speed is the critical factor like multipliers hence DTMOS technology offers higher speed. Transistor count, Transistor size and delay in critical path also affects the speed of the circuit. A 1-bit full adder can be fully characterized by the below equations [6]:

$$Sum = (A \oplus B) \oplus C_{in}$$

$$C_{out} = A \cdot B + (A \oplus B) \cdot C_{in}$$

II. 14-TRANSISTOR FULL-ADDER CELL

The 14-transistor full adder circuit is shown in figure 1, which is implemented using CMOS technology.

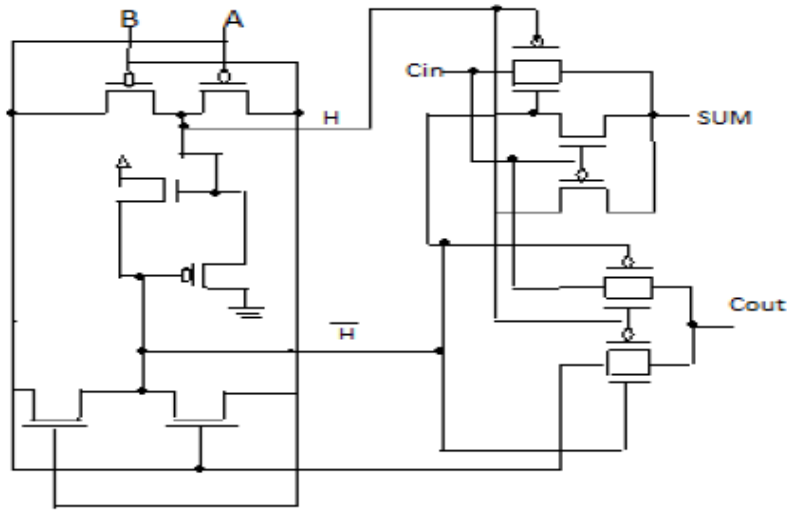

Figure 1: The 14 Transistor Full Adder

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This adder circuit is made using XOR and NOR gates which are implemented using 4 transistors and 2 transistors respectively. NOR gate is used after XOR gate to produce XNOR gate which is used to produce the Sum and carry out. Pass transistor and transmission gates are also used in this structure of full adder[1]. Incomplete voltage swing of the XOR gate when A = B = 0, both the N and P transistors will be ON (N is weakly ON), which will lead to drawing current from the power supply although the circuit is in steady state. Power consumption has increased because of this incomplete voltage swing, but still it remains a good candidate for low power applications due to having only 14 transistors

$$\text{Sum} = H \text{ XNOR } C_{in} = H.C_{in}' + H_o.C_{in}$$

$$C_{out} = A.H_o + H.C_{in}$$

Where H is half adder sum (A XOR B) and H_o is complement of H.

Figure 2 shows the schematic of 14-transistor full adder[3] cell using CMOS technology which has been implemented on Cadence IC 6.1.5.500.14 Virtuoso Simulation tool. The full-adder cell has been simulated in both .18µm & .09µm technology whose average power and delay is been calculated using cadence tool.

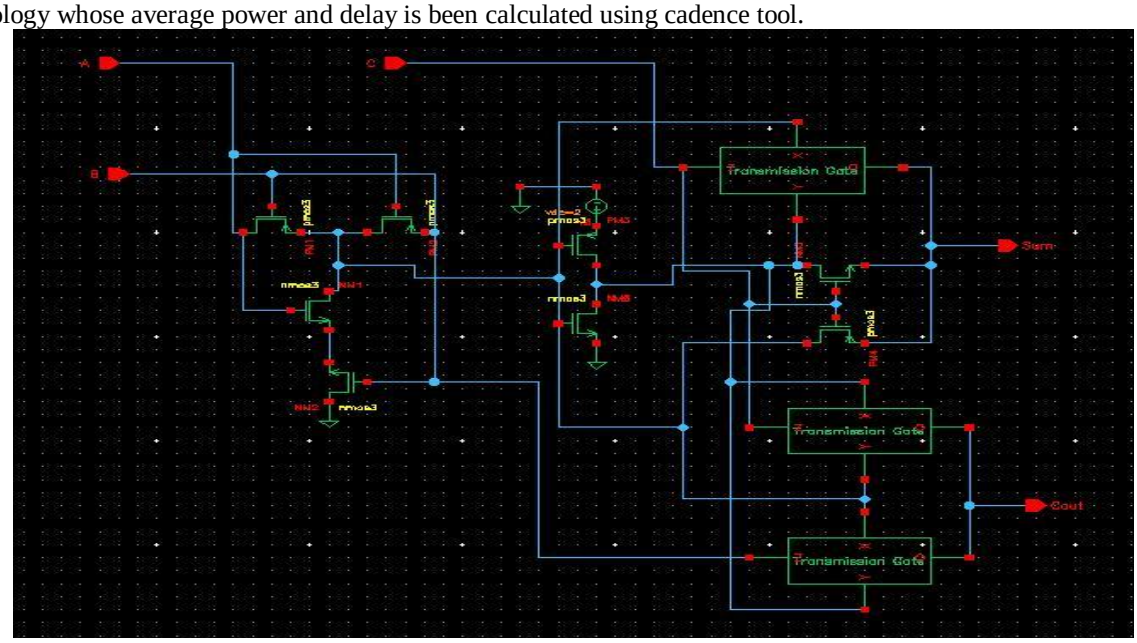

Figure 2: 14 Transistor Full Adder using CMOS Technology

III. 14-TRANSISTOR FULL ADDER USING DTMOS TECHNOLOGY

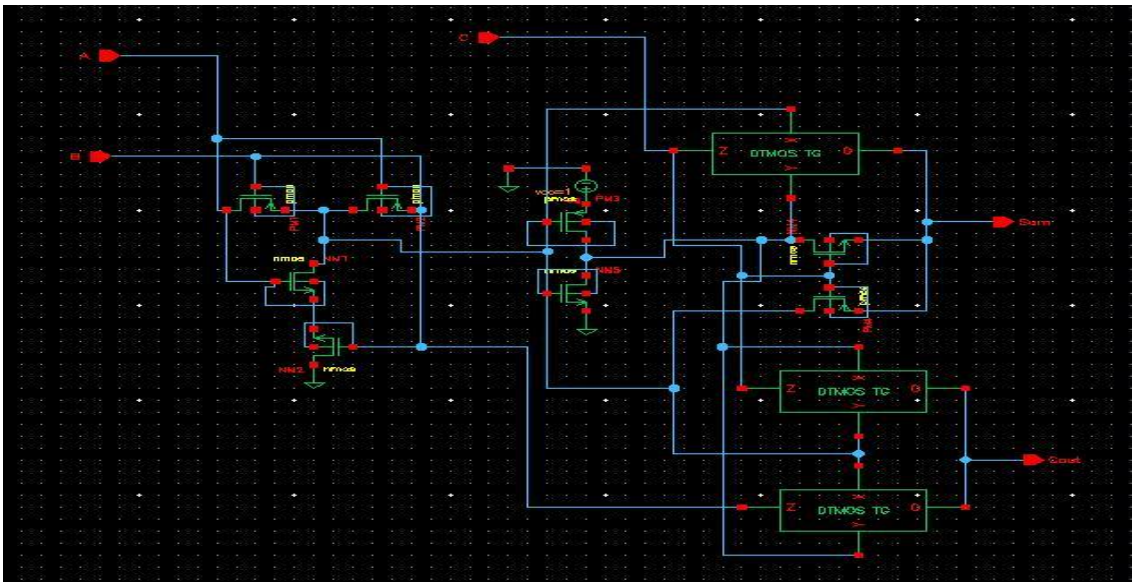

Figure 3: Proposed 1-bit 14-Transistor Full Adder Using DTMOS Technology

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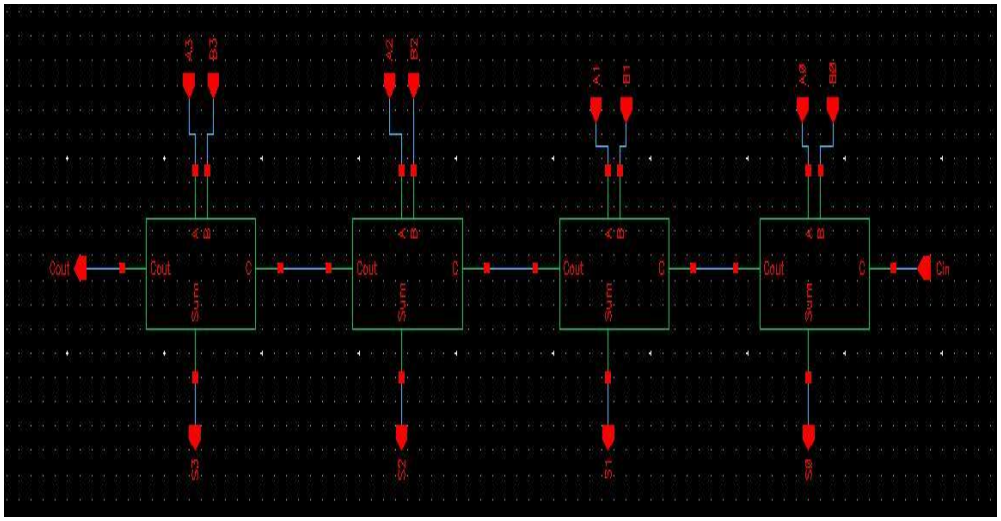

Figure 4: Proposed 4-bit 14-Transistor Full Adder Using DTMOS Technology

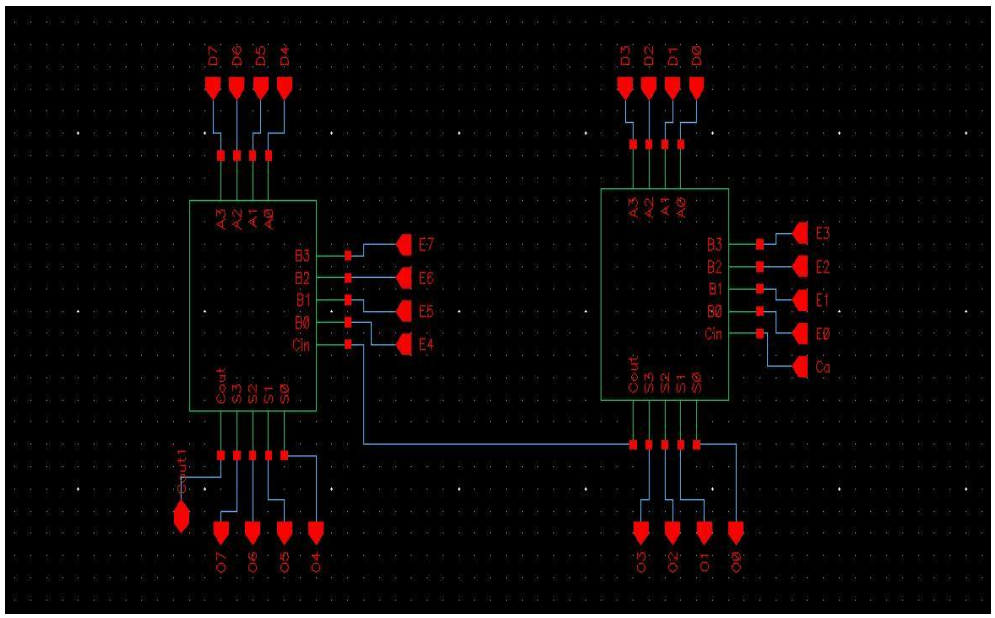

Figure 5:Proposed 8-bit 14-Transistor Full Adder Using DTMOS Technology

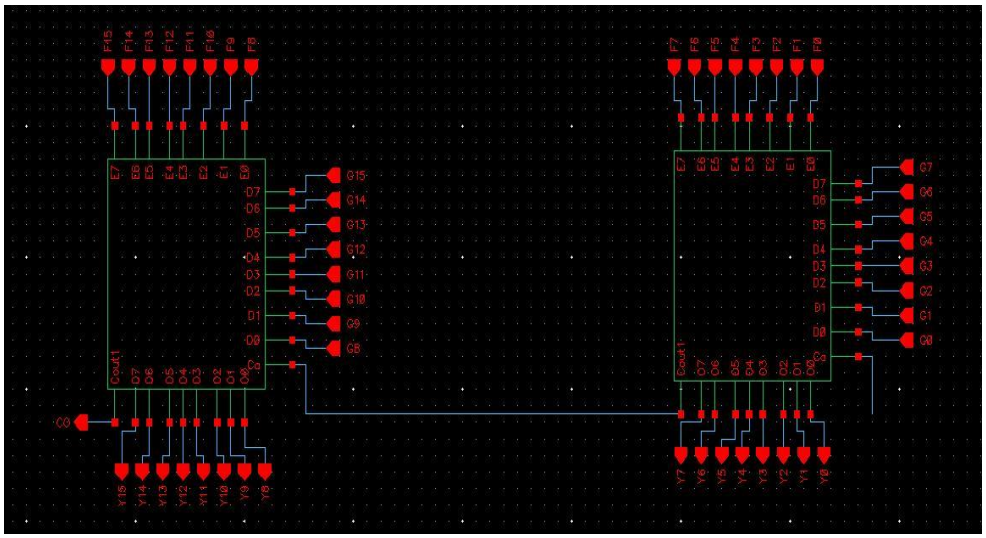

Figure 6: Proposed 16-bit 14-Transistor Full Adder Using DTMOS Technology

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Dynamic Threshold Metal Oxide Semiconductor (DTMOS) is an excellent technique for high speed, low power and low voltage applications. In DTMOS body of the MOSFET is tied to its gate and by applying this technique great many features can be observed. During reverse bias DTMOS provides high threshold voltage which causes low or negligible leakage current. During forward bias it provides low threshold voltage so it is great of high current driving capabilities. DTMOS is a great technology as it is compatible with existing technology and also it does not require any extra circuitry.

Here 14-transistor full adder cell has been implemented using DTMOS technology on Cadence Virtuoso simulation tool using .18µm technology. Figure 3 represents the 1-bit 14 transistor full adder circuit using DTMOS technology. Similarly Figure 4, 5 and 6 represents 4-bit, 8-bit and 16-bit adder circuits implemented using DTMOS technology.

IV. SIMULATION AND RESULT

Simulations have been performed using Cadence Virtuoso tool based on .18µm CMOS technology with different supply voltages. By using different voltage cycles, three inputs are generated which are fed into the adder cell, resulting two outputs are generated at the output of the adder cell. The different Input voltages (V_{dd}) are applied for the conventional CMOS and proposed DTMOS full adder circuits. Table-1 shows the comparison results of CMOS and DTMOS at .18µm.

Table -1 Simulation Result: Variation of Average Power, Propagation Delay and Power delay Product of 14T full adder using DTMOS and CMOS technology at .18µm technology.

Number of Bits	CMOS			DTMOS		
	Average Power (MiliWatts)	Delay (Nano Seconds)	Power Delay Product (Nano Watt-seconds)	Average Power (MiliWatts)	Delay (Nano Seconds)	Power Delay Product (Nano Watt-seconds)
1-bit	217.6	72.76	15.832	243.0	47.9	11.135
4-bit	262.7	41.79	10.978	274.2	33.04	9.059
8-bit	285.0	53.82	15.338	287.9	47.03	13.539
16-bit	222.7	42.09	9.373	235.8	0.34	.080

Dynamic threshold MOS (DTMOS) circuit shows high current driving capabilities in forward bias mode and low leakage currents during zero bias mode. From the above Table 1, It can be concluded that DTMOS has less delay and Power delay product as compared with CMOS but consumes more power than CMOS. DTMOS is an excellent technique to provide less delay with increased speed compared to traditional body biasing in the sub-threshold region.

V.CONCLUSION

The performance of the full adder circuits largely defines the characteristics of the digital VLSI applications. In this paper 1-bit and higher bits 14-Transistor full adder cells have been implemented using DTMOS technology and compared with 14-Transistor CMOS adder cells. Both Adders using .18µm technology has been implemented in cadence tool and from comparison results it can be concluded that the DTMOS adder embodies many advantages over CMOS adder like high speed, lower Power delay product and shows better results at low voltage supply.

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